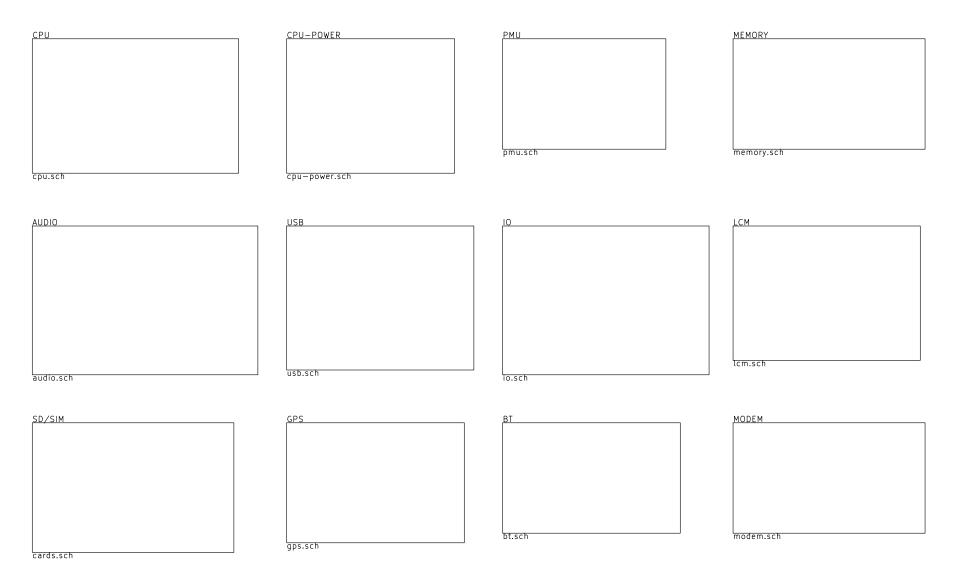
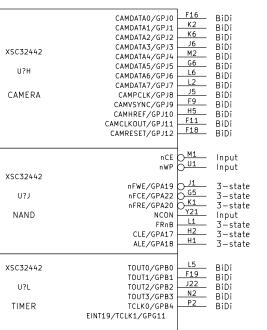
## EXPANDED VIEW - FOR COMPONENT REVIEW

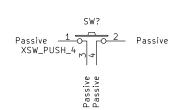




Passive

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X? XTAS4025A

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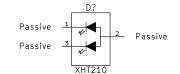
Pwr In

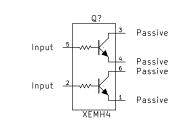
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Pwr In

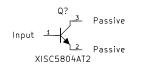
3

Passive





	CAMDATA7/GPJ7	LZ
CAMERA	CAMPCLK/GPJ8	J5
	CAMVSYNC/GPJ9	F 9
	CAMHREF/GPJ10	H5
	CAMCLKOUT/GPJ11	F1:
	CAMRESET/GPJ12	F18
	0,00002	
	nCE	<u>Ь м1</u>
	nWP	<u>6 U1</u>
XSC32442		Ĕ
	nFWE/GPA19	<u>b 11</u>
U?J	nFCE/GPA22	<u>65</u>
	nFRE/GPA20	<u>б к1</u>
NAND	NCON	Y2:
	FRnB	L1
	CLE/GPA17	H2
	ALE/GPA18	H1
XSC32442	TOUT0/GPB0	L5
X3C3Z44Z	TOUT1/GPB1	F19
U?L	TOUT2/GPB2	J22
012	TOUT3/GPB3	N2
TIMER	TCLK0/GPB4	P2
THER	EINT19/TCLK1/GPG11	
	2	
Passive	D? <sup>2</sup> <sup>3</sup> <sup>3</sup> <sup>3</sup> <sup>3</sup> <sup>3</sup> <sup>3</sup> <sup>3</sup> <sup>2</sup> <sup>3</sup>	e
Passive -	R? XR_US Passive	



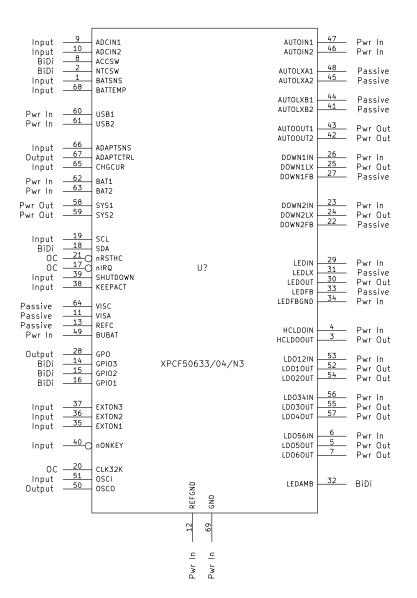
CLOCK	EXTCLK	G22	Input
	CLKOUTO/nSPICSO/GPH9	AA13	BiDi
	CLKOUT1/GPH10	AE14	BiDi
	MPLLCAP	V25	Passive
	UPLLCAP	W25	Passive
	XTIPLL	L25	Input
	XTIPLL	E22	Output
XSC32442	XTIRTC	V26	Input
	XTORTC	W22	Output
U?O	0M0	AE23	Input
	0M1	AB22	Input
	0M2	AA22	Input
	0M3	AE19	Input
DEVICE	CONTROL nBATT_FLT	O <mark>F20</mark>	Input
	PWREN	F20	Output
	nRESET	OH22	Input
	nRSTOUT/GPA21	AE18	Output
JTAG	nTRST	N25	Input
	TCK	E20	Input
	TDI	F22	Input
	TDO	M22	3-state
	TMS	E21	Input
XSC32442 U?D EINT	EINT0/GPF0 EINT1/GPF1 EINT2/GPF2 EINT3/GPF3 EINT4/GPF4 EINT5/GPF5 EINT6/GPF6 EINT7/GPF7 EINT8/GPG0 EINT10/nSS0/GPG2 EINT10/nSS0/GPG2 EINT14/SPIM0S11/GPG5 EINT14/SPIM0S11/GPG5 EINT14/SPIM0S11/GPG6 EINT15/SPICLK1/GPG7 EINT16/CR51/GPG10 EINT19/TCLK1/GPG11 EINT20/GPG13 EINT22/GPG15	T22 U26 N21 T26 R22 U25 K21 T25 AA14 AE15 AB15 AF14 AB14 AB14 AB14 AB14 AB14 AB20 AB20 AB20 AB21 AA19 AF16 W21 AE18	BiDi BiDi BiDi BiDi BiDi BiDi BiDi BiDi
XSC32442		AB12	
U?N	IICSCL/GPE14	U21	BIDI
IIC	IICSDA/GPE15		BIDI
XSC32442 U?K USB	DNO DPO DN1/PDNO DP1/PDPO	AB18 AB17 AA17 AE17	BiDi BiDi BiDi BiDi

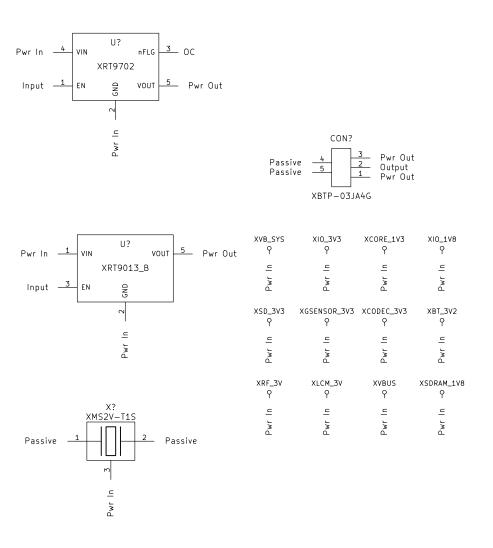
CPU

## CPU-POWER

	A45         A45           A45         Pwr           B21         Pwr           B22         Pwr           B24         Pwr           A25         Pwr           Pwr         Pwr	<u>.</u>		
Pur la T21	VDDIARM VDDIA			
PwrIn <u>Y25</u> PwrIn <u>Y25</u> PwrIn <u>Y22</u>	VDDA_UPLL VDDA_MPLL VDDA_ADC	VDDQ_SDRAM VDDQ_SDRAM VDDQ_SDRAM	AF15 AF10 AF3	Pwr In Pwr In Pwr In
Pwrln <u>K5</u> Pwrln <u>F21</u> Pwrln <u>Y26</u>	VDDALIVE VDDALIVE VDD_RTC	VDDQ_SDRAM VDDQ_SDRAM VDDQ_SDRAM VDDQ_SDRAM VDD_SDRAM	AF23 AF19 AF7 AC2	PwrIn PwrIn PwrIn PwrIn
Pwr         In         AB16           Pwr         In         P21           Pwr         In         N5           Pwr         In         AC1	VDDOP VDDOP1 VDDOP2 VDDOP3	VDD_SDRAM VDD_SDRAM VDD_SDRAM VDD_SDRAM	AE25 AF24 AF13 AF2	Pwr In Pwr In Pwr In Pwr In
	XSC32442 U?P			
Pwr InAA21Pwr InU22Pwr InB22Pwr InH6Pwr InW1Pwr InAA7	VSSOP VSSOP VSSOP1 VSSOP2 VSSOP3 VSSOP3	VSS_SDRAM VSS_SDRAM VSS_SDRAM VSS_SDRAM VSSQ_SDRAM VSSQ_SDRAM	AE2 AF25 AD1 AD26 AF11 AF17 AF9	Pwr In Pwr In Pwr In Pwr In Pwr In Pwr In Pwr In
PwrIn AF20 PwrIn AB26 PwrIn P22	VSSA_ADC VSSA_MPLL VSSA_UPLL	VSSQ_SDRAM VSSQ_SDRAM VSSQ_SDRAM VSSQ_SDRAM	AF22 AF21 AF12 AF6	Pwr In Pwr In Pwr In Pwr In
	V V V V V V V V V V V V V V V V V V V			
	C21         C21           621         621           625         62           625         62           625         62           625         62           625         62           625         62           625         62           625         62           625         62           625         62           625         62           625         62           625         62           71         13           11         14           12         12           13         13           14         14           15         12           16         12           17         14		-	

PMU



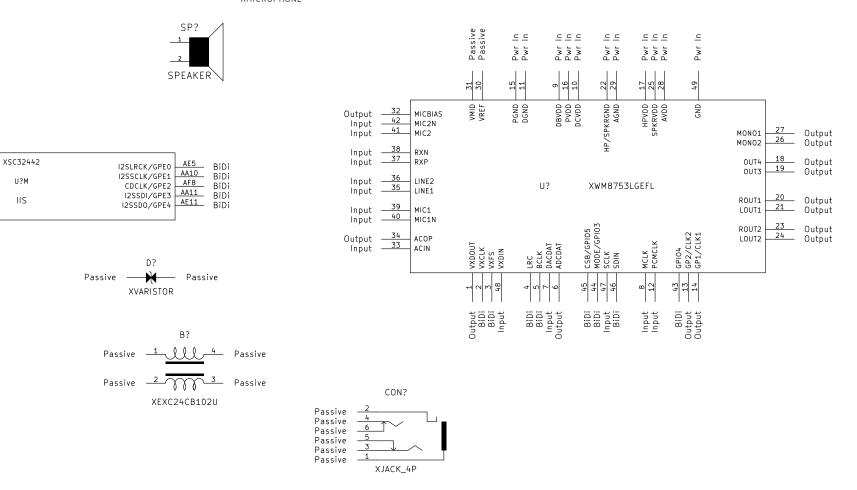


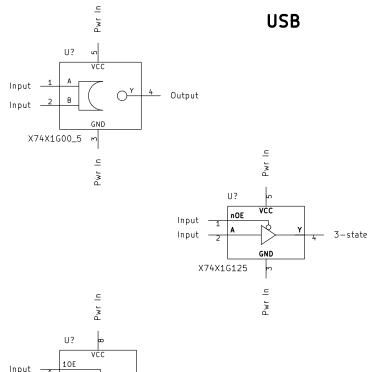
BIDI BIDI	<ul> <li>3-state</li> <li>3-state</li> <li>3-state</li> <li>3-state</li> <li>3-state</li> <li>3-state</li> <li>3-state</li> <li>3-state</li> </ul>	- 3-state BiDi - 3-state - 3-state	MEMORY	
3-state     E11       3-state     B11       3-state     B11       3-state     ADDR0/GPA0       3-state     ADDR1       3-state     D1       ADDR3       3-state     B1       ADDR5       3-state     B1       ADDR6       3-state     ADDR5       3-state     ADDR6       3-state     ADDR6       3-state     ADDR1       3-state     ADDR1       3-state     ADDR1       3-state     ADDR1       3-state     ADR1       3-state     ADR1       3-state     B12       ADDR1       3-state     B12       ADDR1       3-state     B12       ADDR1       3-state     B12       ADDR1       3-state     B13       ADDR12       3-state     B13       ADDR15       3-state     B15       3-state     B15       3-state     B15       3-state     B15       3-state     B15       3-state     F12       ADDR20/GPA5       3-state     B16       ADDR20/GPA5	иссс35/6РА15 <u>102</u> х2с25/6РА13 <u>105</u> посс55/6РА13 <u>105</u> посс55/6РА15 <u>102</u> лосс55/6РА15 <u>102</u> лосс557 <u>102</u> лосс557 <u>102</u> <u>102</u> <u>102</u> <u>102</u> <u>102</u> <u>102</u> <u>102</u> <u>102</u> <u>102</u> <u>102</u> <u>102</u> <u>102</u> <u>102</u> <u>102</u> <u>102</u> <u>102</u> <u>102</u> <u>102</u> <u>102</u> <u>102</u> <u>102</u> <u>102</u> <u>102</u> <u>102</u> <u>102</u> <u>102</u> <u>102</u> <u>102</u> <u>102</u> <u>102</u> <u>102</u> <u>102</u> <u>102</u> <u>102</u> <u>102</u> <u>102</u> <u>102</u> <u>102</u> <u>102</u> <u>102</u> <u>102</u> <u>102</u> <u>102</u> <u>102</u> <u>102</u> <u>102</u> <u>102</u> <u>102</u> <u>102</u> <u>102</u> <u>102</u> <u>102</u> <u>102</u> <u>102</u> <u>102</u> <u>102</u> <u>102</u> <u>102</u> <u>102</u> <u>102</u> <u></u>	Bib         A17         BiDi           DATA0         B19         BiDi           DATA1         B19         BiDi           DATA2         B18         BiDi           DATA2         B18         BiDi           DATA3         B18         BiDi           DATA4         A15         BiDi           DATA2         B18         BiDi           DATA4         A16         BiDi           DATA4         A16         BiDi           DATA4         A16         BiDi           DATA5         A18         BiDi           DATA6         A23         BiDi           DATA1         B23         BiDi           DATA1         B25         BiDi           DATA1         B25         BiDi           DATA1         B25         BiDi           DATA13         B26         BiDi           DATA14         C26         BiDi           DATA15         C26         BiDi           DATA14         C26         BiDi           DATA15         C26         BiDi           DATA16         A24         BiDi           DATA10         C25         BiDi <td><math display="block"> \frac{1}{2} \xrightarrow{7} \frac{6}{5} </math> <math display="block"> \frac{1}{4} \xrightarrow{7} \frac{6}{5} </math> <math display="block"> R_PACK4 </math></td> <td><math display="block">\begin{array}{c c c c c c c c c c c c c c c c c c c </math></td>	$ \frac{1}{2} \xrightarrow{7} \frac{6}{5} $ $ \frac{1}{4} \xrightarrow{7} \frac{6}{5} $ $ R_PACK4 $	$\begin{array}{c c c c c c c c c c c c c c c c c c c $
3-state 3-state 3-state 3-state 3-state 3-state 515 ADDR22/GPA7 ADDR22/GPA8 ADDR24/GPA9 ADDR25/GPA10 ADDR26/GPA11	BiDi <u>N6</u> nxDACK1/GFB7 BiDi <u>P6</u> nxDACK1/GFB7 BiDi <u>R2</u> nxDACK1/GFB8 BiDi <u>T6</u> nxDACK1/GFB8 BiDi <u>T6</u> nxDACK0/GFB10	DATA24 DATA25 DATA26 DATA26 DATA27 DATA27 DATA28 M26 DATA29 P26 BiDi DATA30 DATA31 XSC32442 U?I SDRAM	$\begin{array}{c ccccccccccccccccccccccccccccccccccc$	Input       J8       nCS       XK4M51323PE       DQ25       A1       BiDi         DQ28       B1       BiDi       DQ27       C2       BiDi         DQ27       C2       BiDi       DQ27       C2       BiDi         DQ28       B1       BiDi       DQ29       D2       BiDi         DQ29       D2       BiDi       DQ23       BiDi       DQ30       D3       BiDi         Input       K7       nCAS       nWE       DQ31       E2       BiDi       DQ41       F2       Input         Input       J2       CKE       DQ400       K9       Inpu       Inpu       E2       Inpu         S S S S S S S S S S S S S S S S S S S

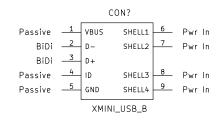
## **AUDIO**

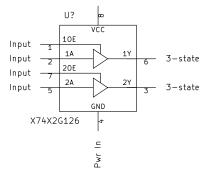
MIC?

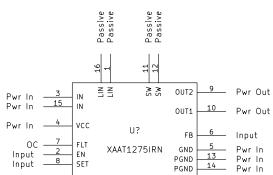


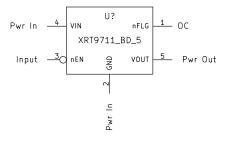


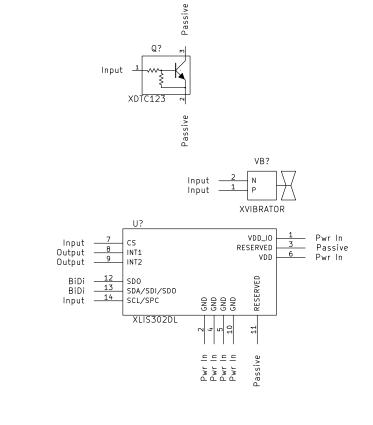




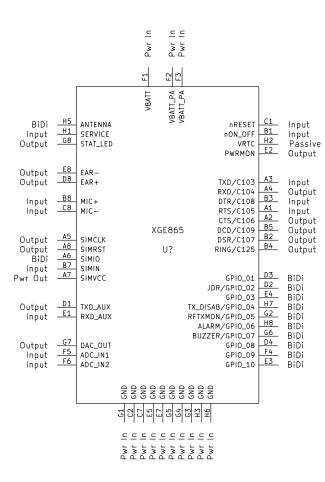








AB10 AA12 AE10	SDCLK/GPE5 SDCMD/GPE6 SDDATO/GPE7	XSC32442
R21	SDDAT0/GPE8	U?B
AE12 AB11	SDDAT2/GPE9 SDDAT3/GPE10	SDIO
AA15 AB13	SPIMISO0/GPE11	
AA16	SPIMOSIO/GPE12 SPICLKO/GPE13	
	VD23/nSS0/GPD15	
	EINT10/nSS0/GPG2	
	EINT20/nSPICS0/GPG12	
	CLKOUT0/nSPICS0/GPH9	XSC32442
	VD16/SPIMIS01/GPD8	X3CJ2442
	EINT13/SPIMIS01/GPG5	U?C
	VD17/SPIMOSI1/GPD9	
	EINT14/SPIMOSI1/GPG6 VD9/SPICLK1/GPD1	SPI
	VD9/SPICLKI/GPD1 VD18/SPICLK1/GPD10	
	EINT15/SPICLK1/GPG7	
	VD22/nSS1/GPD14	
	EINT11/nSS1/GPG3 VD8/nSPICS1/GPD0	
J21	nCTS0/GPH0	
R26	nRTS0/GPH1	
L22 R25	TXD0/GPH2	
	RXD0/GPH3	XSC32442
	EINT17/nRTS1/GPG9	
		U?E
F17	EINT18/nCTS1/GPG10	
F17 P25	TXD1/GPH4	
F17 P25	· · ·	UART
P25 L21	TXD1/GPH4	
P25	TXD1/GPH4 RXD1/GPH5	



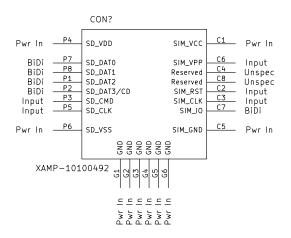
			CON?			
Input Input	Pwr In Pwr In	<u>3</u> 4	VDDIO VDC	VSYNC HSYNC	37 38	Input Input
Input Input Input	Pwr In Pwr In	1 2	LED+ LED-	B0 B1 B2	16 17 18	Input Input
Input Input Input Input	Output Output Output Output	6 7 8 9	YU XL YL XR	82 83 84 85	19 20 21	Input Input Input Input
	Passive	14	NC	G0 G1	22 23 24	Input Input
	Input BiDi Input	10 11 13	XCS DIN SCL	G2 G3 G4 G5	25 26 27	Input Input Input Input
	Input	15	XRES	RO	28 29	Input
	Input		PCLK	R1 R2	30 31	Input Input
	Pwr In Pwr In	<u>12</u> <u>36</u> 34	VSS(GND) VSS(GND)	R3 R4 R5	32 32	Input Input Input
	Pwrln Pwrln	5	VSS(GND) VSS(GND)	DE	39	Input
			XFH23-39S	-0.3SH		

XSC32442 U?F ADC / TSP	AINO     AE20 AIN1     Input       AIN1     AE22 AIN2     Input       AIN3     AC25 AC25     Input       AIN4/YM     AE26 AE26     Input       AIN6/YP     AA25     Input       AIN6/YM     AE25     Input       AIN6/YM     AB25     Input       AIN7/YP     AB25     Input       VREF     AE21     Input
Input 1 Input 2 Input 3 Input 4 XFA2012	2 9 0utput 7 0utput 6 0utput 0utput 0utput 0utput

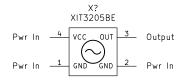
XSC32442 U?G LCD INTERFACE	VD0/GPC8 VD1/GPC9 VD2/GPC10 VD3/GPC11 VD4/GPC12 VD5/GPC13 VD6/GPC14 VD7/GPC15 VD8/nSPICS1/GPD0 VD9/SPICK1/GPD1 VD10/GPD2 VD11/GPD3 VD12/GPD4 VD13/GPD5 VD14/GPD6 VD15/GPD7 VD16/SPIMIS01/GPD9 VD18/SPICK1/GPD10 VD18/SPICK1/GPD10 VD19/GP011 VD20/GPD12 VD21/GPD13 VD22/nS51/GPD14 VD23/nS50/GPD15 LEND/GPC0 VCLK/GPC1 VLINE/GPC2 VFRAME/GPC3	AA6 AA9 V2 Y5 V6 Y1 AB5 W5 AA1 AB1 AB1 AB1 AB1 AB1 AB1 AB1 AB1 AB1	BiDi BiDi BiDi BiDi BiDi BiDi BiDi BiDi
	VM/GPC4		BiDi
	LCD_LPCOE/GPC5		BiDi
	LCD_LPCREV/GPC6	R6	BiDi
	LCD_LPCREVB/GPC7	AA8	BiDi
EINT	12/LCD_PWREN/GPG4		

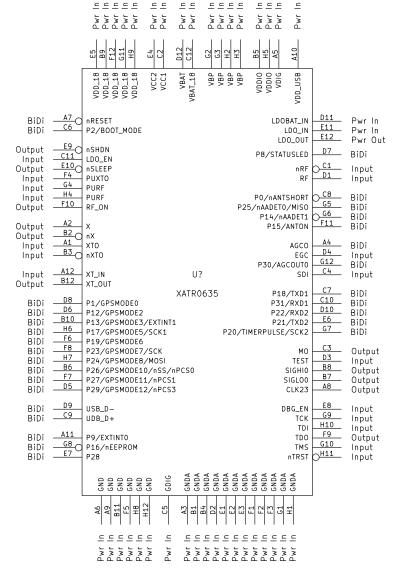
LCM

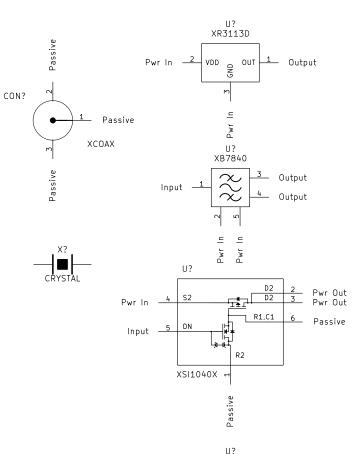
SD/SIM

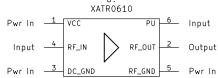


Note: G1 through G6 are called Grounding-I, II, III, IV, V, and VI in the data sheet.









GPS



